SYSTEM DESCRIPTION
VIATRON 2140/2150 GENERAL PURPOSE COMPUTER

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CONTENTS

VIATRON 2140/2150 GENERAL PURPOSE COMPUTERS

VIATRON's 2140/2150 General Purpose Computers provide the user with a versatile data processing tool at surprisingly low cost. In common with all of VIATRON's data management products, the 2140/2150 computers use LSI/MOS circuitry to reduce costs and improve reliability.

Some of the major features of the 2140/2150 computers:

- Low Cost . . . The 2140 sells for $4752 – the 2150 for $9552.
- Extensive Instruction Repertoire . . . Over 85 powerful machine language instructions
- Versatile Addressing Capability . . . direct and indirect addressing as well as address indexing
- Byte Manipulation . . . Reduces user formatting requirements
- Multiprecision Arithmetic Capabilities . . . For complex data computations
- Hardware Multiply and Divide
- Multi-Accumulator Configuration . . . Provided by three 16-bit arithmetic registers and one 16-bit extension register
- Priority Interrupt System . . . Offers up to four interrupt levels
- Easy-to-Operate Program Entry . . . Through low-cost, reusable VIATAPE cartridges
- Automatic Initial Program Load . . . Lets the operator load the program at the touch of a single button
- Complete Software Package . . . Provides an easy-to-use assembler language, simplified report and data manipulating compiler and FORTRAN IV

2140/2150 COMPUTER CHARACTERISTICS

The following tables provide a summary of some of the functional and physical characteristics of the Model 2140/2150 General Purpose Computers.

FUNCTIONAL CHARACTERISTICS

Main Memory	4,096 or 8,192 16-bit words of random access magnetic core storage
Word Length	16-bit basic word
Byte Size	Halfword - 8 bits
Arithmetic Operations	8,16,32 or 48 bits
Instruction Length	Short Format (16-bits) or Extended Format (32-bits).
Addressing	In Short Format, relative addressing with or without indexing In Extended Format, direct or indirect addressing with or without indexing.
General Operating Registers	Three single length (16-bit) registers (A, B, and C) An extension register (Q) A double length (32-bit) register comprising A and Q A triple length (48-bit) register comprising A, B, and Q
Index Registers	Three
Input/Output Subsystem	Program-controlled transfers through three APC's (Automatic Polling Controller), or high-speed direct memory access (DMA) transfers through the high-speed channel.

PHYSICAL CHARACTERISTICS

Height	30 inches
Width	15-1/2 inches
Depth	28 inches
Weight	62 pounds
Volume	7 cubic feet
Clearance Requirements	Mounts flush on rear and sides
Power Requirements	115V ac, 60 Hz, 350 watts Also available for 50 Hz power
	Office ambient
Environmental Requirements	32° F – 96° F Maximum condensing Relative Humidity 98%

2140/2150 COMPUTER ARCHITECTURE

VIATRON's unique approach to computer design has resulted in an efficient computer architecture that provides the user with a simple-to-use-yet powerful-computer.

The 2140/2150 Computers are arranged in five subsystems:

System Bus
Central Processing Unit (CPU)
Main Memory
I/O Subsystem
Operator's Control Panel.

These subsystems and their interrelationships are illustrated in Figure 1.

System Bus

The System Bus, the main data path for all address and data transfers, ties together the Central Processing Unit (CPU), the Main Memory and the Input/Output Subsystems. All data transfers are synchronous 16-bit parallel moves.

Central Processing Unit (CPU)

The CPU is the computing and control center of the 2140/2150 Computers. It consists of a Control Memory, CPU Control and two identically configured Arithmetic Units.

Control Memory

The Control Memory, also referred to as Read Only Memory (ROM), is the nerve center of the computer. Its major function is to select, interpret, and direct the execution of the stored program. In performing this task, the ROM coordinates the various activities of receiving data and transferring processed data to the Input/Output Subsystem for subsequent use by the terminals and peripheral devices.

CPU Control

CPU Control contains logic whose prime function is to direct the operation of the ROM. It receives commands from Core Memory, the Operator's Panel, the I/O Controller, or the ROM itself and then determines the next ROM step.

Arithmetic Units

Arithmetic, logic, and other computational operations performed by the CPU occur within the Arithmetic Units. Basically, each arithmetic unit is composed of an adder, three accumulator registers, and an operand buffer register, each with a 16-bit capacity. These identical units can operate both idenpendently and in conjunction with each other.

Arithmetic Unit I is used primarily for computation and logic manipulation and consists of the A, B, and C registers.

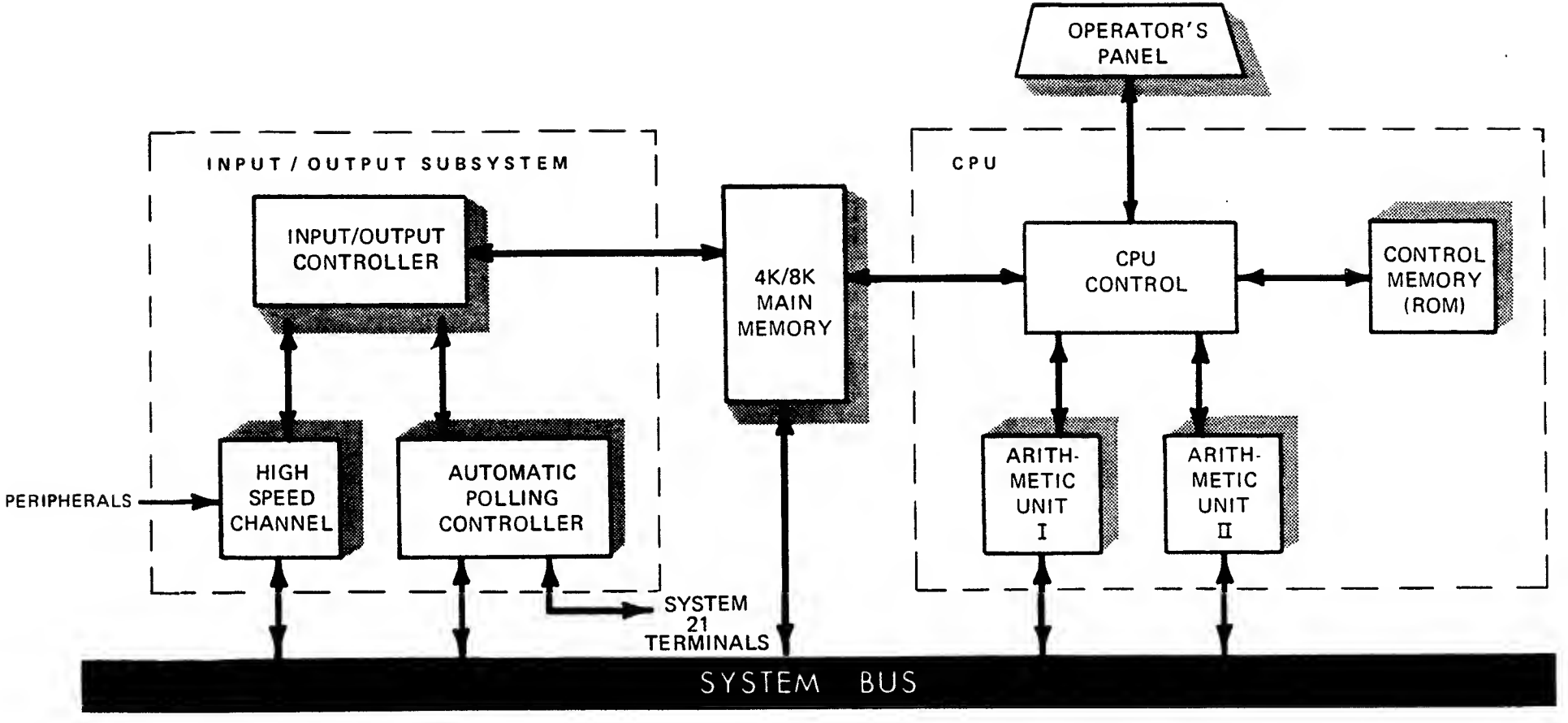

OPERATOR'S PANEL
INPUT / OUTPUT SUBSYSTEM
CPU
INPUT/OUTPUT CONTROLLER
4K/8K MAIN MEMORY
CPU CONTROL
CONTROL MEMORY (ROM)
PERIPHERALS
HIGH SPEED CHANNEL
AUTOMATIC POLLING CONTROLLER
ARITH-METIC UNIT I
ARITH-METIC UNIT II
SYSTEM 21 TERMINALS
SYSTEM BUS

Figure 1

The A, B, and C Registers can perform arithmetic and logic operations such as addition, subtraction, and various Boolean functions. The multiply and divide operations are performed in conjunction with the Q Register of Arithmetic Unit II. Data can be moved between registers or any register can be used as a shift register with a full complement of right-shift and left-shift operations. Data can be transferred to or from the Main Memory in either 16-bit or byte format.

In Arithmetic Unit II, addressing operations can be performed in the P and R Registers and arithmetic in the Q Register.

The P Register is the program counter. The P Register contains the address of the next stored program instruction.

The Q Register, or quotient register, is used as an accumulator extender during arithmetic operations. These include double precision (32-bit) operations when called for by add, subtract, store, or load instructions. Triple precision (48-bit) operations are performed with the A and B Registers assigned the high-order bits and the Q Register processing low-order bits. Q is also the multiplier-quotient register.

The R Register is used during effective address generation and also as an operator's panel address register.

Main Memory

The primary storage facility of the 2140/2150 Computers is the magnetic-core Main Memory. It provides random access, data and instruction storage and retrieval. The Memory has maximum storage capacity of either 4,096 16-bit words in the 2140 Computer, or 8,192 16-bit words in the 2150 Computer.

A data-save feature allows the memory to retain data during power turn-on and shut-down as well as during power-failure conditions.

Input/Output Subsystem

The Input/Output (I/O) Channel Controller manages all requests for data transfer between Main Memory and I/O devices operating with the computer (see Figure 2). The I/O Controller monitors and controls all external requests for memory access initiated by the Automatic Polling Controller (APC) and the high-speed channel. Data transfer takes place as either 8-bit (byte) or 16-bit parallel operations on a request-acknowledge basis.

Direct Memory Access

The Model 2140/2150 Computer Direct Memory Access is provided through the High-Speed Channel, allowing data transfers to or from a peripheral device in a cycle-steal mode. When an I/O device requires a data transfer with memory, it steals a memory cycle from the CPU. Therefore, the controls of the CPU are temporarily halted. Up to eight cycle-stealing devices can be connected to the High-Speed Channel by an optional multiplexer. When used, each device interfaces with the multiplexer through a device controller. The device controller provides a buffer for transferring blocks of data synchronously with memory and asynchronously with the peripheral device. It also contains the necessary counters to supply address information to the memory and to detect end-of-data transfer. The device controller sends 16 bits of status information to memory under program control.

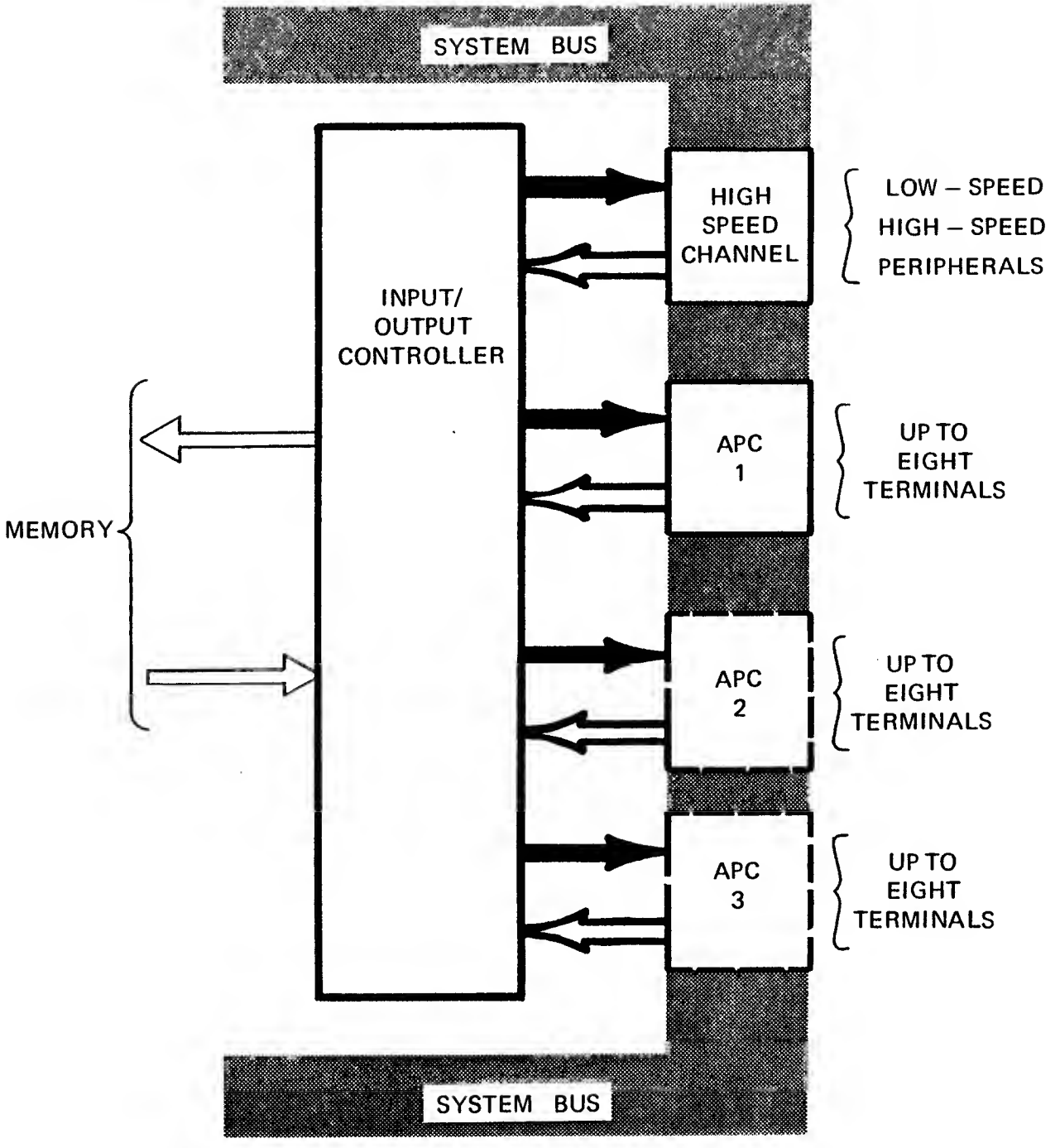

SYSTEM BUS
INPUT/
OUTPUT
CONTROLLER
HIGH
SPEED
CHANNEL
LOW – SPEED
HIGH – SPEED
PERIPHERALS
APC
1
UP TO
EIGHT
TERMINALS
APC
2
UP TO
EIGHT
TERMINALS
APC
3
UP TO
EIGHT
TERMINALS
MEMORY
SYSTEM BUS

Figure 2

Interrupt Priority Levels

Four interrupt levels are a standard feature on the 2140/2150 Computers. These interrupt levels are assigned a priority. The priority logic within the I/O Controller interrupts the current program when it senses that a higher priority interrupt level is requesting service. All lower interrupt levels are locked out until released by the program.

APC Channels

The Automatic Polling Controller (APC) provides the capability of interfacing the computer with up to eight System 21 Data Management Terminals without any field modifications. The APC relieves the I/O Controller from all functions except to monitor priority allocations to the APC, thereby simplifying the operating requirements of the I/O Controller. The Model 2140 Computer has one APC Channel, while the Model 2150 Computer has three APC Channels. Therefore, the Model 2140 Computer can interface with up to eight System 21 Data Management Terminals, while Model 2150 can interface with up to twenty-four Systems 21 Data Management Terminals.

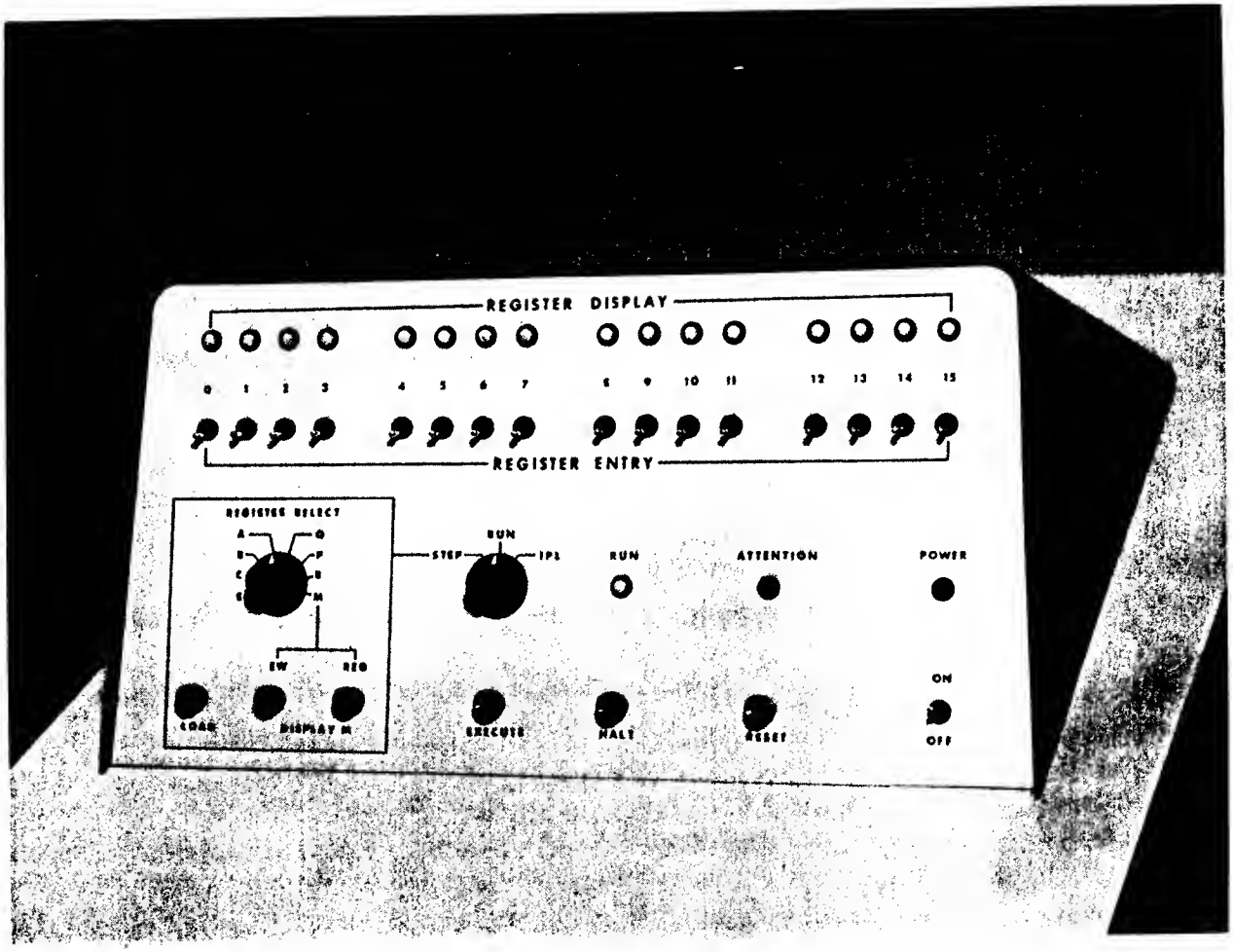
Each APC operates as a polling controller as it sequentially steps, one by one, to a time slot allocated for a specific terminal. Data can be transferred between the computer and a terminal during its assigned time period. The polling process is continuous and allows equal time for each terminal data transfer for a particular APC. This design allows sufficient growth capability to meet all user requirements for distributed data collection.

Operator's Control Panel

The Operator's Control Panel permits the user to monitor and load all of the following:

Any Core Location
Registers A, B, C, P, Q, or R
Carry and Overflow (Status)

The Control Panel is human-engineered for simple operation. An indicator lamp on the panel can be set under program control to alert the operator to an event in the program execution.



Operator's Control Panel for the Model 2140 / 2150 Computer

THE 2140/2150 COMPUTER -- A PROGRAMMER'S VIEW

From a programmer's view, VIATRON's 2140/2150 computers incorporate an ideal mixture of operating registers (3) and index registers (3), as well as a comprehensive and flexible set of instructions.

General Registers

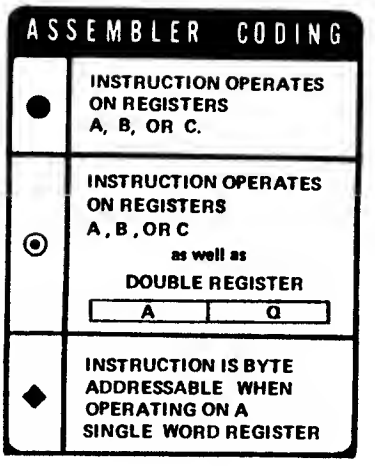
The CPU includes three 16-bit, accumulator-type operating registers, designated A, B, and C. For double-word operations, register D, a combination of registers A and Q (an internal quotient register), is used. For triple-word operations, the triple register comprising registers A, B, and Q is used. Eight-bit bytes are handled through the left-hand portion of register A, B, or C.

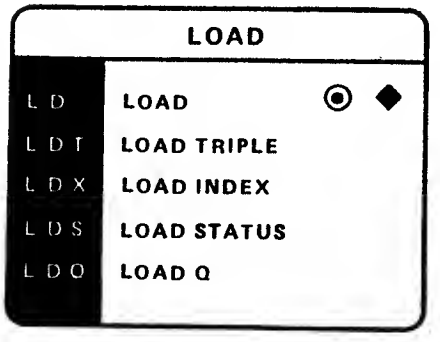
Index Registers

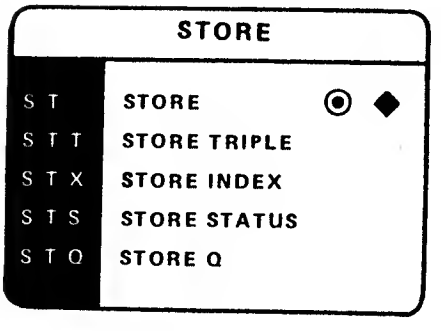
Three index registers are provided. When indexing is selected, the contents of the selected index register are added to the effective address. Several instructions are provided for loading, modifying, and storing the contents of the index register.

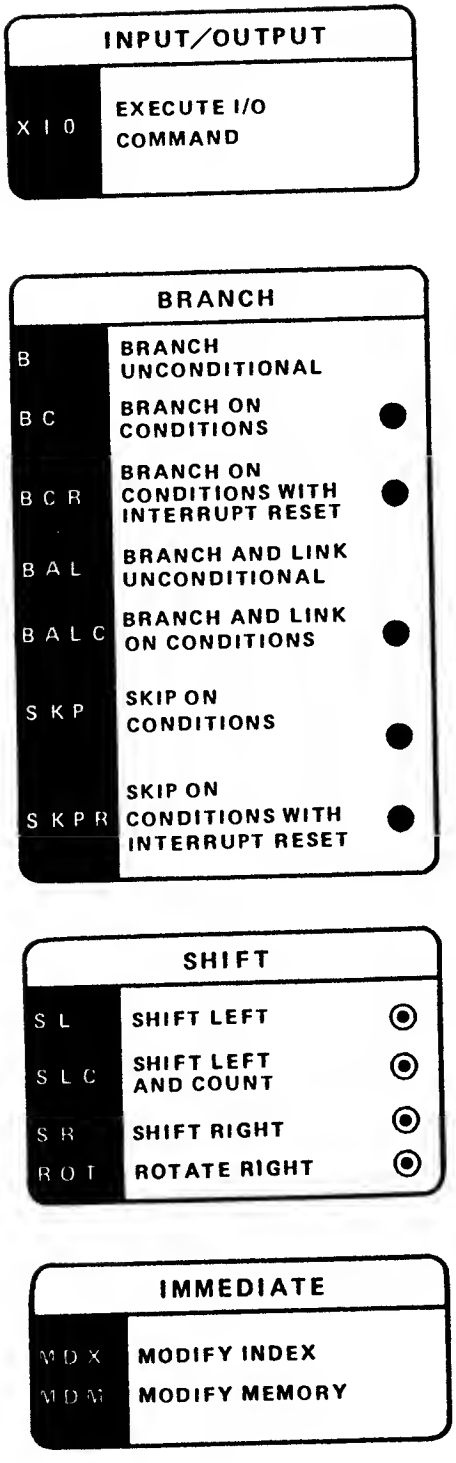
Instruction Set

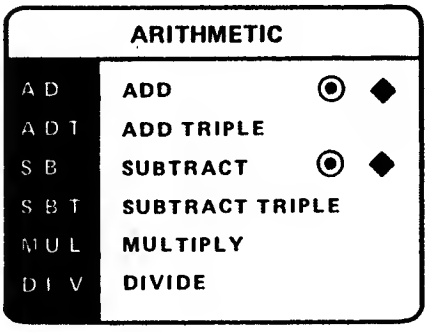
The instruction set for the Model 2140/2150 Computers provides a powerful working set in nine groups as shown below:

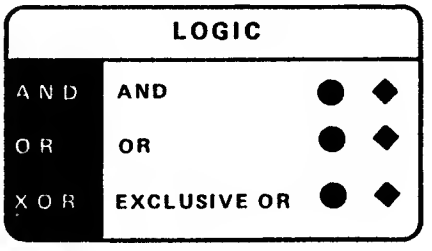


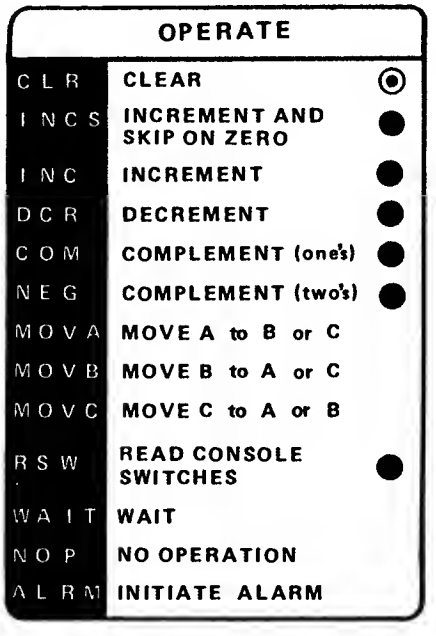





INPUT/OUTPUT
X I O
EXECUTE I/O COMMAND
BRANCH
B
BRANCH UNCONDITIONAL
B C
BRANCH ON CONDITIONS
B C R
BRANCH ON CONDITIONS WITH INTERRUPT RESET
B A L
BRANCH AND LINK UNCONDITIONAL
B A L C
BRANCH AND LINK ON CONDITIONS
S K P
SKIP ON CONDITIONS
S K P R
SKIP ON CONDITIONS WITH INTERRUPT RESET
SHIFT
S L
SHIFT LEFT
S L C
SHIFT LEFT AND COUNT
S R
SHIFT RIGHT
R O T
ROTATE RIGHT
IMMEDIATE
M D X
MODIFY INDEX
M D M
MODIFY MEMORY


ARITHMETIC
AD
ADD
ADT
ADD TRIPLE
SB
SUBTRACT
SBT
SUBTRACT TRIPLE
MUL
MULTIPLY
DIV
DIVIDE


LOGIC
AND
AND
OR
OR
XOR
EXCLUSIVE OR


OPERATE
CLR
CLEAR
INCS
INCREMENT AND SKIP ON ZERO
INC
INCREMENT
DCR
DECREMENT
COM
COMPLEMENT (one's)
NEG
COMPLEMENT (two's)
MOVA
MOVE A to B or C
MOVB
MOVE B to A or C
MOVC
MOVE C to A or B
RSW
READ CONSOLE SWITCHES
WAIT
WAIT
NOP
NO OPERATION
ALRM
INITIATE ALARM

Data Formats

Numerical data is stored in one, two or three 16-bit core locations in (signed) two's complement format. Examples of the formats follow (Figure 3).

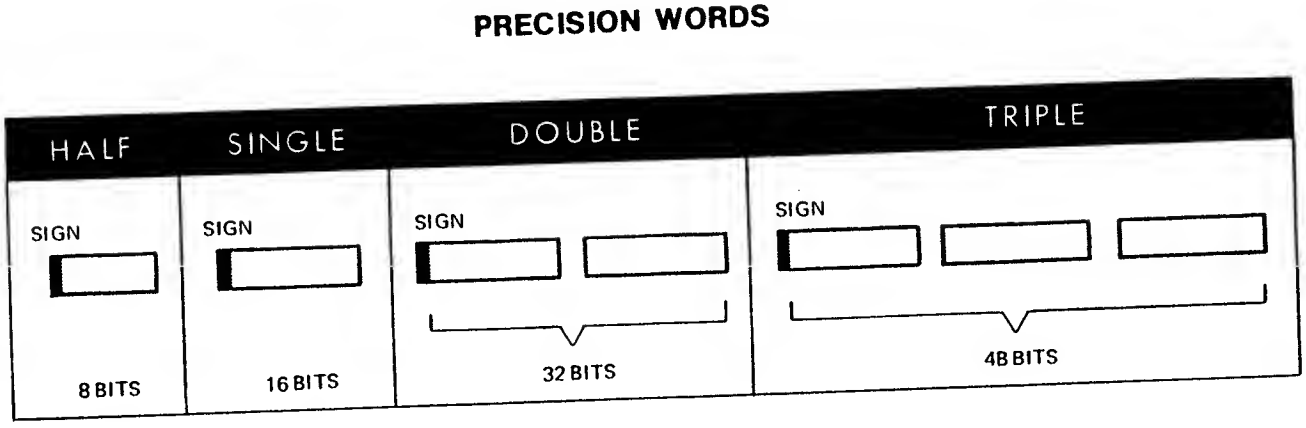


Figure 3

VIATRON Programming System

A comprehensive software package called the VIATRON Programming System (VPS) is available with each System 21 Model 2140/2150 General Purpose Computer. Maximum flexibility and compatibility are achieved by including standardized language processors, utility programs, and system library routines in the VPS.

Language Processors

A vital consideration in evaluating any data processing system is the facility for program preparation. VPS meets this requirement by providing a fully symbolic assembler language, a business-data management language similar to a report generator, and two versions of a standard scientific compiler.

The VIATRON Assembler Language converts readily understood symbolic source language statements into the binary object code used by the computer.

Basic FORTRAN IV (USASI X3.10-1966) and Standard FORTRAN IV (USASI X3.9-1966) are one-pass scientific/mathematical compilers for the 4K Model 2140 General Purpose Computer and the larger 8K Model 2150, respectively.

Distributed Data Language—I (DDL-I) is an ideal terminal-oriented language for generating application systems for general business data processing. Similar to a report generator, it is normally found only in systems costing many times the 2140/2150 computers.

Subroutine Library

The Subroutine Library for the VIATRON Programming System is a package of commonly used routines for data input/output, data conversion, and arithmetic functions. The subroutines required for operation of an object program are selected by the Linkage Editor program when the object program is being processed.

Input/Output Subroutines include a Terminal Master Control Package controlling up to 24 terminals.

A number of Mathematical Function Subroutines are available for use by other programs including:

- Trigonometric sine/cosine
- Trigonometric arctangent
- Square Root
- Natural Logarithms
- Exponentials

Arithmetic subroutines include functions designed to augment the CPU arithmetic instructions. The subroutines perform the functions of floating-point operations (single or double precision) for add, subtract, multiply, and divide.

Utility Program Library

A set of utility routines is available with the VIATRON Programming System for handling object programs stored on VIATAPE cartridges. They include the Core Dump and Linkage Editor Routines and a Subroutine Library Manager.

Dump Routines are used to output the contents of core memory to a System 21 Terminal in hexadecimal form.

The Linkage Editor Routine accepts the binary output of language translators. The Linkage Editor creates a self-loading core-image tape containing the compiled or assembled program and the required subroutines. This facility enables repeated program loadings without further reference to the Subroutine Library.

Subroutine Library Manager Routine allows the user to build, edit, and maintain a relocatable output on the convenient and economical VIATAPE cartridges.

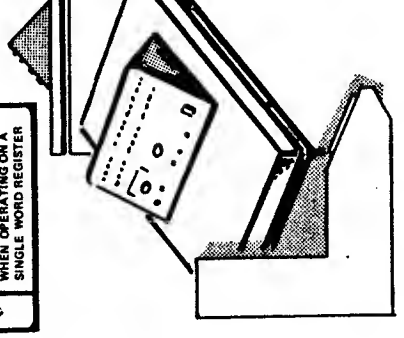
VIATRON

SYSTEM

Model 2140/2150

GENERAL PURPOSE COMPUTER

REFERENCE CARD



ASSEMBLER CODING KEY

●	INSTRUCTION OPERATES ON REGISTERS A, B, OR C.
⊙	INSTRUCTION OPERATES ON REGISTERS A, B, OR C as well as DOUBLE REGISTER (A, Q)
◆	INSTRUCTION IS BYTE ADDRESSABLE WHEN OPERATING ON A SINGLE WORD REGISTER

VIATRON COMPUTER SYSTEMS CORPORATION

CROSBY DRIVE, BEDFORD, MASSACHUSETTS

Printed in U.S.A.

CONDITION TABLE

CHARACTER	CONDITION BRANCH	CONDITION SKIP
Z	ZERO	ZERO
+ or &	PLUS	PLUS
—	MINUS	MINUS
O (ALPHA)	ODD	NOT ODD (EVEN)
C	CARRY	NOT CARRY
V	OVERFLOW	NOT OVERFLOW

TABLE OF POWERS

POWERS OF 16 16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

POWERS OF 2 2^n	n
512	9
1 024	10
2 048	11
4 096	12
8 192	13
16 384	14
32 768	15
65 536	16
131 072	17
262 144	18
524 288	19
1 048 576	20
2 097 152	21
4 194 304	22
8 388 608	23
16 777 216	24

DECIMAL HEX BINARY EQUIVALENTS

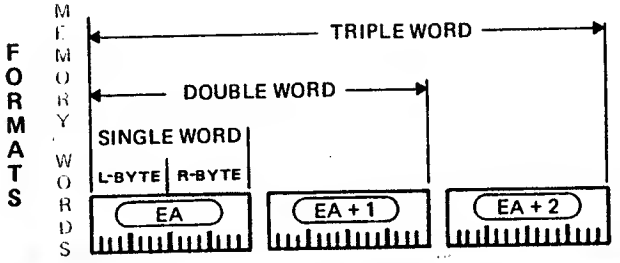
DEC	HEX	BINARY
	1	0001
	2	0010
	3	0011
	4	0100
	5	0101
	6	0110
	7	0111
	8	1000
	9	1001
	A	1010
	B	1011
	C	1100
	D	1101
	E	1110
	F	1111
1		0001
2		0010
3		0011
4		0100
5		0101
6		0110
7		0111
8		1000
9		1001
10		1010
11		1011
12		1100
13		1101
14		1110
15		1111

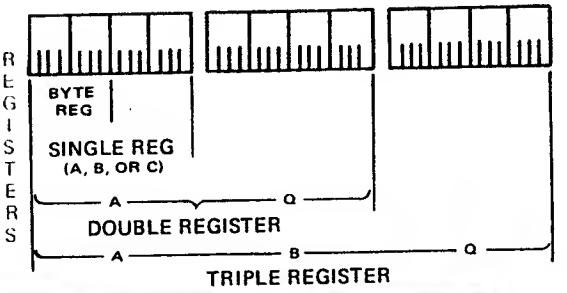
HEXADECIMAL AND DECIMAL CONVERSION

HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
	4		3		2		1
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

8

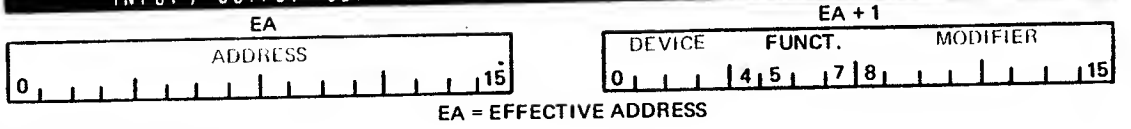
FORMATS





7

INPUT / OUTPUT CONTROL COMMAND FORMAT



EA = EFFECTIVE ADDRESS

LABELS

* COL 21: COMMENT

COL 21 MUST BE A THRU Z, $, ., #, OR @:

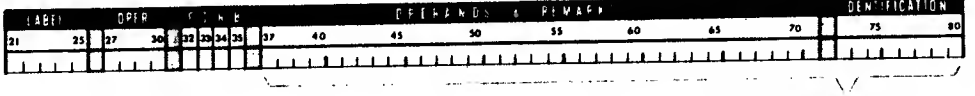
the remaining columns may be any legitimate character - spaces are not permitted except at right end.

INDEXING

(BLANK) or 0: PROGRAM COUNTER
1: INDEX REG 1
2: INDEX REG 2
3: INDEX REG 3

BYTE DESIGNATION

(BLANK): WHOLE WORD
L: LEFT BYTE (0)
R: RIGHT BYTE (1)



6

FORMAT

(BLANK): SHORT WITH RELATIVE DISPLACEMENT
D: SHORT WITH ABSOLUTE DISPLACEMENT
E: EXTENDED AND DIRECT
I: EXTENDED AND INDIRECT

REGISTERS

(BLANK): REGISTER A
A: REGISTER A
B: REGISTER B
C: REGISTER C
D: DOUBLE A D

OPERANDS

*: THIS LOCATION FOLLOWING IS HEX
/: FOLLOWING IS A CHARACTER VALUE
.:

+: PLUS
−: MINUS
*: MULTIPLICATION

BLANKS ARE NOT PERMITTED; ALL INFORMATION FOLLOWING A BLANK IS NOT ASSEMBLED BUT IS LISTED AS A REMARK

ES041

LOAD

	LOAD
T	LOAO TRIPLE
X	LOAD INDEX
S	LOAD STATUS
Q	LOAD Q

STORE

	STORE
T	STORE TRIPLE
X	STORE INDEX
S	STORE STATUS
Q	STORE Q

ARITHMETIC

	ADO
T	AOO TRIPLE
	SUBTRACT
T	SUBTRACT TRIPLE
L	MULTIPLY
V	DIVIDE

LOGIC

AND	AND
OR	OR
XOR	EXCLUSIVE OR

OPERATE

CLR	CLEAR
INCS	INCREMENT AND SKIP ON ZERO
INC	INCREMENT
DCR	OECREMENT
COM	COMPLEMENT (one's)
NEG	COMPLEMENT (two's)
MOVA	MOVE A to B or C
MOVB	MOVE B to A or C
MOVC	MOVE C to A or B
RSW	REAO CONSOLE SWITCHES
WAIT	WAIT
NOP	NO OPERATION
ALRM	INITIATE ALARM

INPUT/OUTPUT

XIO	EXECUTE I/O COMMANO

BRANCH

B	BRANCH UNCONDITIONAL
BC	BRANCH ON CONOITIONS
BCR	BRANCH ON CONOITIONS WITH INTERRUPT RESET
BAL	BRANCH AND LINK UNCONOITIONAL
BALC	BRANCH ANO LINK ON CONOITIONS
SKP	SKIP ON CONOITIONS
SKPR	SKIP ON CONDITIONS WITH INTERRUPT RESET

SHIFT

SL	SHIFT LEFT
SLC	SHIFT LEFT AND COUNT
SR	SHIFT RIGHT
ROT	ROTATE RIGHT

IMMEDIATE

MDX	MODIFY INOEX
MDM	MODIFY MEMORY

PROGRAM CONTROL

ABS	ABSOLUTE ASSEMBLY
ORG	DEFINE ORIGIN
END	END OF PROGRAM

DATA DEFINITION

DC	OEFINE CONSTANT
DEC	DECIMAL DATA
XFLC	EXTENOEO FLOATING CONSTANT
ASCI	ALPHANUMERIC CONSTANT

STORAGE ALLOCATION

BSS	BLOCK STARTEO BY SYMBOL
BES	BLOCK ENDED BY SYMBOL

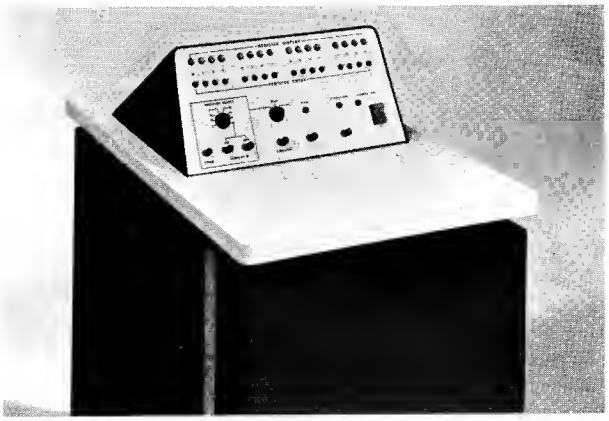
SYMBOL DEFINITION

EQU	EQUATE SYMBOL

PROGRAM LINKING

ENT	SUBROUTINE ENTRY POINT
ISS	INTERRUPT SERVICE ENTRY POINT
CALL	CALL SUBROUTINE
CDB	CALL OATA BLOCK

General-Purpose Computers



MODEL 2140

The VIATRON Model 2140 is an LSI/MOS Central Processing Unit with a 4096 16-bit word core memory. It offers extensive computational and data manipulation capabilities through 85 powerful instructions.

Arithmetic operations may be single, double or even triple precision using general purpose registers (accumulators) which are available to the programmer. Computational routines may therefore be easily programmed for the simplest or the most complex business or scientific calculations. Load, Store, Move and Test instructions may also be performed in all three registers and may be byte or word oriented.

Software available with the 2140 will be upwards compatible with future VIATRON computers. The software includes a Basic FORTRAN compiler, an assembler, a math subroutine library and utility programs for manipulating data from System 21 Data Management Terminals. In addition, a language for communicating with multiple data management terminals is available in DDL-1 (Distributed Data Language). This gives the user a powerful systems capability by supplying software control of terminals.

The input/output capability is accomplished through an Automatic Polling Controller, which allows the attachment of up to 8 System 21 Data Management Terminals, and a wideband high speed data channel, which may be used for data communications and computer peripherals. System 21 terminals may, of course, be configured to support any of the terminal peripherals in the System 21 product line, adding extensive data input, data storage, data display, and data printout capabilities to the Model 2140 computer.

An operator's control panel, designed for simplicity of operation, is located at desk height on the Model 2140. It allows access to all machine registers for display or for direct storage from the panel.

MODEL 2150

The Model 2150 expands the capability of VIATRON's general-purpose computers to serve more terminals and a wider variety of applications.

More Memory 8192 16-bit words of core memory are standard on the Model 2150, twice the core capacity of the Model 2140. Larger, more complex programs and more on-line data storage are available to the programmer and to the user.

More System 21 Terminals Three Automatic Polling Controllers are standard on the Model 2150, permitting the attachment of up to 24 System 21 Data Management Terminals. With more memory and more terminals, the Model 2150 is ideal for use in large data input centers, in private wire communications networks for message switching, for data transmission to computer centers, and a host of other terminal-oriented application areas.

More Software A FORTRAN IV Compiler is standard on the Model 2150, bringing to the engineer, the scientist, and the mathematician a language which is both familiar and easy to use. For the engineer, or group of engineers, who has been concerned by the high cost and inflexibility of commercial time sharing services, or who has been unable to gain access to his centralized batch processing computer, the Model 2150 offers a cost saving, efficient alternative. Put the computer where the problems are for maximum accessibility and utility.

Specifications

- **Type of Circuitry for CPU:** LSI/MOS
- **Memory:** Magnetic Core
- **Memory Capacity:** 2140: 4096 words
  2150: 8192 words
- **Word Length:** 16 bits (Byte addressable)
- **Memory Cycle Time:** 2 microseconds
- **Index Registers:** 3
- **General-Purpose Registers:** 6
- **Register Length:** 16 bits
- **Interrupt Levels:** 2140: 2
  2150: 4
- **Input/Output:** Automatic Polling Controller
  2140: 8 channels for attaching System 21 Terminals
  2150: 24 channels for attaching System 21 Terminals
  High-Speed Data Channel
- **Data Format:** 8 bit byte — ASCII
  16 bit word
  Arithmetic: 8, 16, 32, or 48 bit numbers
  Positive Numbers: sign and magnitude
  Negative Numbers: 2's complement
- **Instruction Formats:**

Short(S)

0 5	6 7	8 15
6 Bits Op Code	2 Bits Index	8 Bits Relative Address

Extended(E)

0 5	6 7	8 15	16 31
6 Bits Op Code	2 Bits Index	8 Bits Op Code Modifier	16 Bits Address

- **Addressing Modes:**
  Short Format Instructions: 256 Locations relative to Program Counter, and Indexable
  Extended Format Instructions: Direct (Full Memory) Indirect, and Indexable
- **Instructions:**

Arithmetic:	12	Shift:	13
Logic:	9	Modify Memory:	1
Load:	13	I/O:	1
Store:	13	Operate:	12
Branch:	11		—
		Total	85

- **Software**

2140	2150
Assembler	Assembler
Distributed Data Language—1	Distributed Data Language—1
Basic FORTRAN	FORTRAN IV
Subroutine Library	Subroutine Library
Utility Library	Utility Library

- **Power Requirements:** 115 VAC, 60 cycle, 350 watts

price list

Model Feature Number Code	Description	Purchase Price
2101	**MICROPROCESSOR** • 512-word, Read-Only Memory • 400-character Read/Write Memory • Two Tape Channels • Automatic Skip • Automatic Duplication • Automatic Left Zero Fill • Automatic Upper and Lower Shift Control • Automatic Output to selected data or tape channel	$960
101	**AUTOMATIC MULTIPLE INPUT feature** • One record from Selected Channel or medium • One master and one control record from Tape Channel #1	$432
102	**AUTOMATIC MULTIPLE OUTPUT feeture** • To Data Channel 1 and Tape Channel 2 • To Data Channels 1 and 2 • To Data Channels 1 and 2, plus Tape Channel 2 feature	$192
103	**SHORT RECORD feature** • Automatic input or output of a record less than 80 characters. • A "carriage return" character is used to designate end of record.	$480
106	**SHORT RECORD feature** • Automatic input or output of a record less than 80 characters. • A "line feed" character is used to designate end of record.	$480
2111	**MICROPROCESSDR** • 1024-word, Read-Only Memory • 400-character Read/Write Memory • Two Tape Channels • Automatic Skip • Automatic Duplication • Automatic Left Zero Fill • Automatic Upper and Lower Shift • Automatic Output to selected data or tape channel • Automatic Input from selected data or tape channel • Automatic Tape Search • Automatic Tape Validation • Editing, Automatic Reformatting • Key Verification	$1728
102	**AUTOMATIC MULTIPLE OUTPUT feature** • To Data Channel 1 and Tape Channel 2 • To Data Channels 1 and 2 • To Data Channels 1 and 2, plus Tape Channel 2	$192
103	**SHORT RECORD feature** • Automatic input or output of a record less than 80 characters. • A "carriage return" character is used to designate end of record.	$480
104	**AUTOMATIC MULTIPLE INPUT feature** • One master and one control record from Tape Channel 1 • One master and two control records from Tape Channel 1 • Automatic Input from selected data or tape channel, followed by Automatic Output to selected data or tape channel. • Automatic Input from selected data or tape channel to master record, followed by automatic selection of the record area indicated by the Status Record switch.	$432
105	**FIELD AND PDSITION SELECT feature** • Direct Access to selected field or character position	$240
106	**SHORT RECORD feature** • Automatic input or output of a record less than 80 characters. • A "line feed" character is used to designete end of record.	$480

Model Feature Number Code	Description	Purchase Price
2140	**GENERAL PURPOSE COMPUTER** • CPU—4K words of core memory • 16-bit words • 8 Input/Output channels for local or remote attachment of System 21 Data Management Terminals • Wideband Communications channel • Software, Utility subroutines, Assembler, and MACRO languages	$4752
2150	**GENERAL PURPOSE COMPUTER** • CPU—8K words of core memory • 16-bit words • Hardware Multiply and Divide • 24 Input/Output channels for local or remote attachment of System 21 Data Management Terminals • Wideband Communications channel • Software, Utility subroutines, FORTRAN compiler, Assembler, and MACRO languages	$9552
3001	**VIDEO DISPLAY SUBSYSTEM** • Allows the attachment of several types of video displays to a microprocessor	$240
301	**BLACK & WHITE VIDEO DISPLAY** • 320-character display, divided into four 80-character records • Suppression or display of any or all records • Cursor in operational record • Interleaving capability of Write and Master records (No charge for first Black & White Video Display when Feature 304 is not ordered.)	$384
302	**RECORD SUPPRESS feeture** • Permanent suppression of any combination of 80-character records on local or remote displays	$96
303	**SELECTED DATA DISPLAY feature** • Allows selective distribution of data to local or remote displays	$192
304	**COLOR VIDEO DISPLAY** • Requires Selected Date Display feature 303 • 320-character display, divided into four 80-character records • Suppression or display of any or all records • Cursor in operational record • Interleaving capability of Write and Master Records • Control characters for 8 Data and 8 Background Colors	$1248
305	**BLACK & WHITE RF MODULATOR** • Connection for up to 12 RF displays. Displays may be VIATRON Displays (Feature Code 306) or any commercial television display • Up to two RF Modulators may be connected to Microprocessor	$96
306	**BLACK & WHITE RF VIDEO DISPLAY**	$384
KEYBOARDS (prices include Parallel Data Channel at $48)		
4001	**KEYBOARD** • Standard typewriter charecters • Standard card punch characters • Microprocessor control characters • Communications control characters	$288
4002	**KEYBOARD** • Standard typewriter characters • Standard card punch characters • Microprocessor control characters • Communications control characters • 40-character card reader	$624
4099	**KEYBOARD** • Microprocessor control characters	$192
TAPE RECORDERS		
5001	**VIATAPE CARTRIDGE RECORDER** • Capstan-free tape recorder using magnetic tape cartridges • 7-level ASCII code • Bit read/write rate of 1250 bps	$192
5002	**COMPUTER-COMPATIBLE TAPE RECORDER** • 9-track, 800 bpi • 6-inch minireels of computer-competible tape • 2200 cps synchronous read/write rate	$2880
5003	**COMPUTER-COMPATIBLE TAPE RECORDER** • 7-treck, 556 bpi • 6-inch minireels of computer-compatible tape • 2200 cps synchronous read/write rete	$2880

Model Feature Number Code	Description	Purchase Price
501	**800 BPI DENSITY feeture**	N/C
502	**SPACE INSERTION feeture** • In write mode invalid charecters are replaced by space characters instead of a question mark character.	N/C
DATA CHANNEL ATTACHMENTS (prices include Serial Data Channel at $48)		
6001	**CARD READER/ PUNCH ADAPTER** • Transmit any of the card punch's standard 64 characters • Punches an 80-character record in 4.5 seconds • Cerd punch may be disengaged and operated independently	$1776
601	**RECORD TRANSFER BUFFER** • 80-character buffer permitting simultaneous microprocessor operation and card punch operation	$864
602	**BUFFER SHORT RECDRD feature** • For Buffered Units Only • Fixed-length short record • Program card is set up with a skip field. Cerd is released as soon as skip is detected	$96
603	**SPACE INSERTION feature** • In punch mode, adapter spaces over an illegal character instead of punching a question mark	$144
6002	**PRINTING ROBOT** • For IBM Selectric®, 13" Carriage • Includes Format Control • Printing speed of 12 cps • Easily removed for normal typewriter operation • Automatic backspace, tab, carriage return, and index by code detection in data stream • Three print modes for straight line or formetted printing • Upper and lower case	$1200
601	**RECORD TRANSFER BUFFER** • 80-character buffer permitting simultaneous microprocessor operation and printing robot operation	$864
608	**ADAPTER—15" SELECTRIC CARRIAGE**	N/C
6003	**COMMUNICATIONS ADAPTER** • High/Low speed selection 110 and 247 BAUD • 103A2-Compatible • Asynchronous communicetion in half-duplex mode • 7-level, ASCII code, record synchronization, optional parity check, 15-second time out	$528
604	**UNATTENDED OPERATION feeture**	$240
605	**MODEM 110-247 BAUD**	$480
606	**ACOUSTIC COUPLER** • Data transmission up to 300 bps • Includes modem	$720
6004	**COMMUNICATIONS ADAPTER** • High/Low speed selection—600 and 1200 BAUD • 202 C/D-Competible • Asynchronous communication in half-duplex mode • 7-level, ASCII code, record synchronization, optional parity check, 15-second time out	$528
604	**UNATTENDED OPERATION feature**	$240
607	**MODEM 600-1200 BAUD**	$960
6005	**COMMUNICATIONS ADAPTER** • Single special speed up to 1200 BAUD • 103A2- or 202 C/D-Compatible • Asynchronous communication in half-duplex mode • 7-level ASCII code, record synchronization, optional parity check, 15-second time out	$1008
6006	**FOREIGN DEVICE ATTACHMENT** • Allows the input and output of ASCII code foreign devices to the microprocessor • Parallel transfers to and from foreign device	$864
6007	**FOREIGN DEVICE ATTACHMENT** • Allows the input and output of Hollerith code foreign devices to and from the microprocessor • Perallel transfers to and from foreign device	$1104
6008	**UNIT CARD READER** • Hollerith code	$1200
6009	**COMPUTER ADAPTER** Model 2140 & 2150	$576